PCT/AU03/01117

REC'D 07 OCT 2003
WIPO PCT

PRIORITY DOCUMENT
SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)

Patent Office
Canberra

I, JONNE YABSLEY, TEAM LEADER EXAMINATION SUPPORT AND SALES hereby certify that annexed is a true copy of the Provisional specification in connection with Application No. 2002951291 for a patent by ENERGY STORAGE SYSTEMS PTY LTD as filed on 09 September 2002.

COMMONWEALTH OF AUSTRALIA
AUSTRALIA
PATENT OFFICE

WITNESS my hand this
Thirtieth day of September 2003

J R Yabsley

JONNE YABSLEY
TEAM LEADER EXAMINATION
SUPPORT AND SALES

AUSTRALIA

PATENTS ACT 1990

PROVISIONAL SPECIFICATION

FOR THE INVENTION ENTITLED:-

"A POWER SUPPLY"

The invention is described in the following statement:-

FIELD OF THE INVENTION

The present invention relates to a power supply.

The invention has been developed primarily for use with a GPRS communications module for a PCMCIA card and will be described hereinafter with reference to that application. It will be appreciated, however, that the invention is not limited to that particular field of use and is also suitable for other communications modules such as a GSM module or a Mobitex module, whether included in a PCMCIA card, a Compact Flash card, or any other communications module for a notebook computer, a laptop computer, a Tablet computer, a wireless LAN device or other computing devices.

BACKGROUND ART

Known mobile communications modules, such as GPRS modules, are used in PCMCIA cards. The modules include a number of integrated circuits that collectively function to allow information to be processed and transmitted in accordance with the required communications standard. In the case of GPRS modules the information is usually non-voice data, although voice data is transmitted similarly.

The design of portable computing devices such as laptop computers and PDA's is strongly driven to minimise size while maximising the period between recharging of the battery. This suggests that the battery should have as high an energy density as possible. However, batteries of this type typically have a high time constant and are therefore compromised in their ability to provide the required voltage and current during the high power mode of the typical communications modules used in these devices. Accordingly, the more usual compromise is to tolerate a lower power density – and therefore a shorter battery life – but gain a shorter time constant.

In partial answer to this problem, it has been known to use a bank of parallel tantalum capacitors to assist the battery during the high power mode. While some small advantage is gained, this is usually not justified by the cost and bulk of these capacitors.

The design of wireless communication devices for wireless LANs, PCMCIA cards and the like, is driven to achieve the desired functionality while also minimising volume, peak power consumption and cost. In contrast, the demands for increased functionality and wider bandwidth communication usually require more volume, higher peak power and higher cost. These competing considerations place an increased premium on PCB

"real estate", packaging volumes and component costs as designers attempt to get more from less.

In any event, these cards are reliant upon the host computing device supplying the required power. Increasingly it is being found that the host has a specified current limit for the card that is less than the peak current demanded. That is, for the card to operate it will have to do so outside the power supply specification of the host. While this may not be catastrophic in all cases, it is highly undesirable and, ultimately, unsustainable if system stability is required.

Accordingly, for both portable and mains supplied devices the increasing demands for communication flexibility is being compromised and hindered, if not prevented, by power supply limitations.

Any discussion of the prior art throughout the specification should in no way be considered as an admission that such prior art is widely known or forms part of common general knowledge in the field.

DISCLOSURE OF THE INVENTION

It is an object of the invention, at least in the preferred embodiment, to overcome or substantially ameliorate one or more of the disadvantages of the prior art, or at least to provide a useful alternative.

According to a first aspect of the invention there is provided a power supply for a load that demands an average load current and a peak load current that is higher than the average load current, the power supply including:

input terminals for connecting with a power source that supplies a source current that is less than a predetermined current limit, wherein the predetermined current limit is less than the peak load current;

output terminals for electrically connecting with the input terminals and the load; and

a supercapacitor device in parallel with the terminals for allowing the load to be supplied the peak load current while maintaining the source current at less than the predetermined current limit.

Preferably, the predetermined current limit is between the average load current and the peak load current.

Preferably also, the voltage at the input terminals is greater than or equal to the voltage at the output terminals. More preferably, the power supply maintains the input and the output terminals at substantially the same voltage.

In a preferred form, the supercapacitor device includes one or more supercapacitors in parallel with the output terminals. More preferably the power supply includes a current limiter disposed between the input terminals and the supercapacitor device. Even more preferably, the current limiter maintains the source current at less than the predetermined current limit during charging of the supercapacitive device from the power source.

Preferably, the supercapacitor device includes a plurality of supercapacitors that are connected in parallel with each other. However, in other embodiments the supercapacitors are connected in series with each other.

Preferably also, the supercapacitor device has an ESR of less than 30 mΩ. More preferably, the supercapacitor device has an ESR of less than 24 mΩ. Even more preferably, the supercapacitor device has an ESR of less than 20 mΩ.

In a preferred form, the supercapacitor device provides a capacitance of at least about 0.4 Farads. More preferably, the footprint of the device is less than about 800 mm^2. Even more preferably, the footprint of the device is less than about 40 mm x 20 mm.

Preferably, load is a communications device. More preferably, the communications device includes a GPRS module or a GSM module. Even more preferably, the load is a card for a computer, and the communications device is mounted to the card. In these embodiments the power source is derived from the internal power supply of the computer.

According to a second aspect of the invention there is provided a communications card for a computer, the computer having a power source that provides a source current for the card that is less than a predetermined current limit, the card including:

a substrate for supporting a plurality of electrical components that collectively define a load that demands a peak load current that is greater than the predetermined current limit and an average load current that is less than the peak load current;

input terminals for connecting with the power source;

output terminals for electrically connecting with the input terminals and the load; and

a supercapacitor device in parallel with the terminals for allowing the load to be supplied the peak load current while limiting the source current to less than the predetermined current limit.

According to a third aspect of the invention there is provided a computing device including:

a communications card for allowing the computer to communicate with other computing devices wherein, in use, the card demands a peak load current and an average load current that is less than the peak load current;

a power source for supplying a source current to the card, the power source having a predetermined current limit that is less than the peak load current;

input terminals for connecting with the power source;

output terminals for electrically connecting with the load; and

a supercapacitor device in parallel with the terminals for allowing the load to be supplied the peak load current while limiting the source current to less than the predetermined current limit.

The term "computer" includes both mains connected and portable computing equipment such as, for example, desktop computers, laptop computers, PDA's and cellular telephones. The term "card" includes, for example, CompactFlash Cards, PCMCIA cards, modem cards and other communications cards.

BRIEF DESCRIPTION OF DRAWINGS

Preferred embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 is a schematic circuit diagram of a power supply according to the invention;

Figure 2 is a more detailed circuit diagram of the current limit circuit used in the power supply of Figure 1;

Figure 3 is an oscilloscope image including a number of traces for the power supply of Figure 1;

Figure 4 is an oscilloscope image including a number of traces for an alternative embodiment of a power supply according to the invention;

Figure 5 is a schematic representation of a PCMCIA card of one embodiment of the invention; and

Figure 6 is a schematic representation of an alternative communication card according to the invention.

PREFERRED EMBODIMENTS OF THE INVENTION

Referring to Figure 1 there is illustrated schematically a power supply 1 for a load in the form of a PCMCIA card 2 that has an onboard GPRS Class 10 module (not shown). The module, and therefore card 2, demands a load current i_{load} that has an average value over time and periodic instantaneous peak values (i_{peak}) that are significantly higher than the average value. Power supply 1 includes a pair of input terminals 3 for connecting with a power source in the form of a regulated power supply 4 that is contained within a personal computer (not shown). Supply 4 supplies a source current i_{input} that is less than a predetermined current limit specified for the supply and which is less than the peak load current. A pair of output terminals 5 is electrically connected with terminals 3 and card 2. A supercapacitor device in the form of a single supercapcitor 6 is in parallel with terminals 3 and 5 for allowing the load to be supplied the peak load current while maintaining the source current at less than the predetermined current limit.

Power supply 4 has a specification that sets the predetermined current limit at 1 Amp for each card within the computer. In other embodiments the predetermined current limit is different.

It will be appreciated by those skilled in the art that card 1 is but one of a number of cards within the computer, where those cards offer respective functionalities for the user of the computer. For the GPRS functionality, however, a usual GPRS transmitter needs 1.5 Amps to 2 Amps to transmit at full power at the regulated supply voltage of 3.3 Volts. For example, when transmitting in class 10 using a maximum of two of the eight 577 ms time slots, the pulse duration is 1.154 ms and the period 4.616 ms. It is not possible for prior art cards to supply this load and remain within specification. In the embodiment illustrated in Figure 1, however, supercapacitor 6 has a high capacitance and a low ESR (equivalent series resistance) and is thereby able to deliver large current pulses without large voltage swings at terminals 5. That is, the ripple in V_{load} is small and allows the load current i_{load} to meet the peak current demands of card 2 during transmission. In these circumstances i_{load} exceeds the predetermined current limit, while i_{input} does not. That is, supply 1 has a load-levelling effect that allows current drawn from the source 4 during the load pulses to be contained within the range allowed by the PC card specification.

An important criterion in selecting supercapacitor 6 is low ESR, as ESR is typically the major contributor to the voltage ripple for high capacitance devices. However, when card 2 is first plugged into supply 4, supercapacitor 6 is usually in a discharged state. Accordingly, the lower the ESR the higher will be the initial charging current into supercapacitor 6. To prevent the supercapacitor's initial charging current from overloading supply 4, supply 1 includes a current-limit circuit 7. This circuit limits i_{input} to just less than the peak current supply that is specified for card 2. A more detailed illustration of circuit 7 is provided in Figure 2. It will be appreciated by those skilled in the art that during normal operation – that is, following the initial charging of supercapacitor 6 – circuit 7 is effectively inoperative and presents only minimal impedance.

Supercapacitor 6 enables card 2 and the GPRS module to operate even though i_{load} during the periodic peak times exceeds the value allowed by supply 4. This is done with substantially 100% efficiency, instead of the lower efficiency and higher cost of a DC-DC converter. Additionally, supercapacitor 6 does not generate EMI. That is, it is the action of supercapacitor 6 that limits the peak current load upon source 4 during normal operation of card 2. Circuit 7, during that normal operation, is not used to effect that current limiting. Stating this in different terms, supercapacitor 6 is designed to limit i_{input} during normal usage to not only fall below the specification of supply 4, but also to prevent circuit 7 from activating.

The amount of energy that supply 4 is able to deliver in a typical pulse period is able to be compared with the energy required by card 2 by performing a simple energy balance. If the load has a duty cycle of D (where $0 < D \leq 1$) and the load current has a continuous component of I_{steady} and a pulse of i_{peak} (in addition to I_{steady}) then the average power drawn during one cycle is:

$$P_{ave} = V_{cc} (I_{steady} + D \cdot i_{peak})$$

The maximum average power that may be drawn from the supply is given by

$$P_{ave,\,max} = V_{cc} \cdot I_{max}$$

where I_{max} is given by the PC Card specification as 1Amp. P_{ave} must be less than $P_{ave,\,max}$ for the load to function. Combining the above equations, the following must be satisfied:

$$I_{steady} + D \cdot i_{peak} < I_{max}$$

While this equation is true for an ideal, infinite capacitor, some margin is allowed for voltage ripple in a real device. For the illustrated embodiment, the GPRS module is run in Class 10 mode on card 2. Use is made of 2 slots out of 8 to provide a 25% duty cycle, and the card draws 100 mA continuously plus 1.9 Amps peak pulse transmission current. Given this, $I_{steady} + D \cdot i_{peak} = 0.1 + 0.25 \cdot x\ 1.9$ Amps = 0.575 Amps, which is well under the 1Amp limit. This ignores losses, but gives an approximate magnitude of the current that will be drawn from supply 4.

The oscilloscope image of Figure 3 illustrates the traces for the circuit of Figure 1. The x-axis is in units of time, while the y-axis is in units of voltage for the top two traces and current for the bottom two traces.

Supercapacitor 6 is a 0.25 Farad 40 mΩ device. The supply voltage V_{cc} from supply 4 is 3.3 Volts at a supply impedance of 200mW. A load is imposed by card 2 of a 1.9A pulse for 1.154 ms every 4.616 ms. That is, a Class 10 (2-slot) transmission. Progressing from the top to the bottom of the traces provided in Figure 3, there is shown:

1. The input voltage, that is, V_{cc} – designated by reference numeral 11.
2. The load voltage, that is, V_{load} – designated by reference numeral 12.
3. The current drawn from supply 4, that is, i_{input} – designated by reference numeral 13.
4. The current drawn by the GPRS module, that is, i_{load} – designated by reference numeral 14.

It should also be noted that zero is the bottom graticule in the traces.

Due to the use of supply 1 there is no point in the cycle where i_{input} exceeds the 1 Amp specification of supply 4. Moreover, this is achieved simultaneously with i_{load} satisfying the peak current demands of card 2.

It is of interest to note that increasing the impedance of supply 4 or adding resistance to circuit 7 results in a reduced peak input current. However, the tradeoff is a reduced minimum and average output voltage.

The table below, Table 1, contains some examples of supercapacitors that work in the above example with a 2 Amp maximum load current.

In other embodiments use is made of supercapacitors, or supercapacitor devices, with a total ESR of up to 80 mΩ. It will be appreciated, however, from the teaching herein, that those supercapacitors or supercapacitor devices with lower ESR will perform better in the context of the present embodiments, and will also provide more headroom.

An important criterion in selecting supercapacitor 6 is low ESR, as ESR is typically the major contributor to the voltage ripple for high capacitance devices. However, when card 2 is first plugged into supply 4, supercapacitor 6 is usually in a discharged state. Accordingly, the lower the ESR the higher will be the initial charging current into supercapacitor 6. To prevent the supercapacitor's initial charging current from overloading supply 4, supply 1 includes a current-limit circuit 7. This circuit limits i_{input} to just less than the peak current supply that is specified for card 2. A more detailed illustration of circuit 7 is provided in Figure 2. It will be appreciated by those skilled in the art that during normal operation – that is, following the initial charging of supercapacitor 6 – circuit 7 is effectively inoperative and presents only minimal impedance.

Supercapacitor 6 enables card 2 and the GPRS module to operate even though i_{load} during the periodic peak times exceeds the value allowed by supply 4. This is done with substantially 100% efficiency, instead of the lower efficiency and higher cost of a DC-DC converter. Additionally, supercapacitor 6 does not generate EMI. That is, it is the action of supercapacitor 6 that limits the peak current load upon source 4 during normal operation of card 2. Circuit 7, during that normal operation, is not used to effect that current limiting. Stating this in different terms, supercapacitor 6 is designed to limit i_{input} during normal usage to not only fall below the specification of supply 4, but also to prevent circuit 7 from activating.

The amount of energy that supply 4 is able to deliver in a typical pulse period is able to be compared with the energy required by card 2 by performing a simple energy balance. If the load has a duty cycle of D (where $0 < D \leq 1$) and the load current has a continuous component of I_{steady} and a pulse of i_{peak} (in addition to I_{steady}) then the average power drawn during one cycle is:

$$P_{ave} = V_{cc}\,(I_{steady} + D \cdot i_{peak})$$

The maximum average power that may be drawn from the supply is given by

$$P_{ave,\,max} = V_{cc} \cdot I_{max}$$

where I_{max} is given by the PC Card specification as 1Amp. P_{ave} must be less than $P_{ave,\,max}$ for the load to function. Combining the above equations, the following must be satisfied:

$$I_{steady} + D \cdot i_{peak} < I_{max}$$

While this equation is true for an ideal, infinite capacitor, some margin is allowed for voltage ripple in a real device. For the illustrated embodiment, the GPRS module is run in Class 10 mode on card 2. Use is made of 2 slots out of 8 to provide a 25% duty cycle, and the card draws 100 mA continuously plus 1.9 Amps peak pulse transmission current. Given this, $I_{steady} + D \cdot i_{peak} = 0.1 + 0.25 \cdot x\ 1.9$ Amps = 0.575 Amps, which is well under the 1Amp limit. This ignores losses, but gives an approximate magnitude of the current that will be drawn from supply 4.

The oscilloscope image of Figure 3 illustrates the traces for the circuit of Figure 1. The x-axis is in units of time, while the y-axis is in units of voltage for the top two traces and current for the bottom two traces.

Supercapacitor 6 is a 0.25 Farad 40 mΩ device. The supply voltage V_{cc} from supply 4 is 3.3 Volts at a supply impedance of 200mW. A load is imposed by card 2 of a 1.9A pulse for 1.154 ms every 4.616 ms. That is, a Class 10 (2-slot) transmission. Progressing from the top to the bottom of the traces provided in Figure 3, there is shown:

1. The input voltage, that is, V_{cc} – designated by reference numeral 11.
2. The load voltage, that is, V_{load} – designated by reference numeral 12.
3. The current drawn from supply 4, that is, i_{input} – designated by reference numeral 13.
4. The current drawn by the GPRS module, that is, i_{load} – designated by reference numeral 14.

It should also be noted that zero is the bottom graticule in the traces.

Due to the use of supply 1 there is no point in the cycle where i_{input} exceeds the 1 Amp specification of supply 4. Moreover, this is achieved simultaneously with i_{load} satisfying the peak current demands of card 2.

It is of interest to note that increasing the impedance of supply 4 or adding resistance to circuit 7 results in a reduced peak input current. However, the tradeoff is a reduced minimum and average output voltage.

The table below, Table 1, contains some examples of supercapacitors that work in the above example with a 2 Amp maximum load current.

In other embodiments use is made of supercapacitors, or supercapacitor devices, with a total ESR of up to 80 mΩ. It will be appreciated, however, from the teaching herein, that those supercapacitors or supercapacitor devices with lower ESR will perform better in the context of the present embodiments, and will also provide more headroom.

Those supercapacitors listed in Table 1 that are rated for 2.3 Volts operation, two are combined in series for use with supply 4 given the operational voltage is 3.3 Volts. Where lower operational voltages are used a single one of the supercapacitors is suitable. Moreover, in higher voltage applications more than two supercapacitors are connected in series.

TABLE 1

Capacitance (Farads)	ESR (mΩ)	Voltage (Volts)	Footprint (mm x mm)	Thickness (mm)	Type No.
0.18	60	4.5	28.5 x 17	2.79	GW202
0.35 (each)	30 (each)	2.3	28.5 x 17	1.36	GW102 (2 req'd)
0.2	50	4.5	39 x 17	2.06	GS203
0.4 (each)	26 (each)	2.3	39 x 17	0.99	GS103 (2 req'd)

In other embodiments (not shown) card 2 includes a communications module in the form of a GPRS Class 12 module. While the principle of operation remains the same, the parameters of the supercapacitor used are different to account for the requirements of the different module. For example, it is possible to run a transmitter in class 12 mode on a PC Card using four slots out of eight, which is a 50% duty cycle. If the card draws 100 mA continuously plus 1.8 Amps peak pulse transmission current then $I_{steady} + D \cdot i_{peak} = 0.1 + 0.5 \times 1.8$ Amps = 1.0 Amp, which is at the 1 Amp limit. This ignores losses, so a 1.8 Amp pulse is the maximum that could be supported in an ideal circuit. In a real circuit, the pulse load that can be supported will necessarily be less, and the preferred design parameter is 1.5 Amps. Such a 1.5 Amp pulse results in an average of 0.85 Amps, which leaves some headroom and allowance for losses.

An embodiment of the invention that is specifically designed for operation with a PC card having a GPRS Class 12 module includes a superacapacitor that has a capacitance of 0.48 Farads and and ESR of 20mΩ. Again, the source voltage (V_{cc}) is 3.3 Volts and supply 4 provides 200mΩ source impedance. A class 12 (4-slot) transmission includes about a 100 mA continuous load, and a 1.5 Amp maximum pulse for 2.308 ms every 4.616 ms. There is shown in Figure 4 a set of oscilloscope traces that correspond with the traces of Figure 3, but which relate to a GPRS Class 12 module together with the supercapacitor referred to immediately above. That is, progressing from the top trace to the bottom trace, there is illustrated:

1. The input voltage, that is, V_{cc} – designated by reference numeral 15.

2. The load voltage, that is, V_{load} – designated by reference numeral 16.
3. The current drawn from supply 4, that is, i_{input} – designated by reference numeral 17.
4. The current drawn by the GPRS module, that is, i_{load} – designated by reference numeral 18.

Again, due to the use of the supercapacitor i_{input} does not exceed the 1 Amp specification and the load voltage V_{load} remains above 3V.

Adding extra source resistance is a means to reduce the maximum current drawn from supply 4, but it is not advisable in applications in which V_{load} is close to the acceptable minimum.

Examples of supercapacitors that are suitable for use with the GPRS Class 12 module referred to above are listed in Table 2. The design parameters being assumed are a 1.6 Amp maximum load current and that V_{load} is maintained above 3 Volts.

Similarly with the Class 10 examples, the lower the resistances and the ESR of the supercapacitor used, the better the ripple voltage will be and the more voltage headroom there will be.

TABLE 2

Capacitance (Farads)	ESR (mΩ)	Voltage (Volts)	Footprint (mm x mm)	Thickness (mm)	Type No.
0.45	24	4.5	39 x 17	3.9	GS205
0.95 (each)	12 (each)	2.3	39 x 17	1.91	GS105 (2 req'd)
1.4	20	4.5	39 x 17	4.99	GS208
2.7 (each)	10 (each)	2.3	39 x 17	2.46	GS108 (2 req'd)

The invention is also applicable to other operating environments such as CompactFlash Cards including a GPRS or a GSM modem. These cards are typically limited to a current drain of 0.5 Amps, which at a supply voltage of 3.3 Volts, is considerably less than the 1.5 to 2 Amps that the modem requires to transmit at full power. The arrangement is conceptually similar to Figure 1, where card 2 represents the CompactFlash Card including the modem, and supercapacitor 6 represents a supercapacitor selected for this environment.

To illustrate this additional embodiment reference is made to the following specific example. Particularly, the modem is configured to transmit in class 8 mode on a CF+ Card, using 1 slot out of 8, which translates to a 12.5% duty cycle. The card draws

100 mA continuously, plus 1.9 Amps peak pulse transmission current. Using the above equations, $I_{steady} + D \cdot i_{peak} = 0.1 + 0.125 \cdot x\ 1.9$ Amps = 0.34 Amps, which is well under the 0.5 Amp limit. This calculation ignores losses, but gives an approximate magnitude of the current that will be drawn from the source when using a supercapacitor.

The supercapacitor used in this embodiment has a capacitance of 0.25 Farad and an ESR of 40mΩ. Supply 4 provides a source voltage V_{cc} of 3.3 Volts and has a source impedance of about 200 mΩ. The CompactFlash Card draws about 100 mA continuous and a 1.65 Amp pulse for 0.577 ms every 4.616 ms due to the Class 8 (1-slot) transmission. It will be appreciated that the peak source current in practice is higher than the ideal value predicted above, but this is to be expected when taking source resistance and supercapacitor ESR into account.

In other embodiments where CompactFlash Cards are used, the supercapacitor is chosen to have a lower ESR than that used in the above example to allow for some headroom and/or to support a transmitter that draws a higher current.

The table below, Table 3, contains examples of supercapacitors that are also suitable for the embodiments having CompactFlash Cards. These devices allow the load to stay within specification by drawing less than the 0.5 Amp limit. Again, where the specified voltage of the listed supercapacitors is less than the operational voltage of the application, then two like devices are connected in series.

TABLE 3

Max i_{load} (Amps)	Capacitance (Farads)	ESR (mΩ)	Voltage (Volts)	Footprint (mm x mm)	Thickness (mm)	Type No.
1.75	0.45	24	4.5	39 x 17	3.9	GS205
1.75	0.95	12	2.3	39 x 17	1.91	GS105 (2 req'd)
1.65	0.35	32	4.5	28.5 x 17	4.63	GW210
1.65	0.65	16	2.3	28.5 x 17	2.28	GW110 (2 req'd)

Reference is now made to Figure 5 where there is illustrated a PCMCIA card 19. This card conforms to the standard dimensions and is configured for insertion into a complementary port of a desktop computer 20, a laptop computer 21 and a PDA 22. It will be appreciated that such a card or a like card is also able to be fitted to other computing devices.

Card 19 includes a communications module to provide the computing device into which it is installed to communicated with a remote system. It also includes a power supply in accordance with the invention (not shown) to ensure that card 19 remains within specification while the communication is affected.

In other embodiments, however, the power supply according to the invention is mounted within computer 20 or 21 or PDA 22 and not directly to card 19.

Another embodiment of the invention, in the form of a communications card 23, is illustrated in Figure 6. Card 23 is configured for mounting within a computer or other computing device, and includes a GPRS module (not specifically shown) and a power supply according to the invention (also not specifically shown). The usual current drain limit on such a device is 1 Amp notwithstanding the 1.5 to 2 Amp peak requirement of the GPRS module. However, card 23 is able to remain within specification through inclusion of a power supply according to the invention.

Although the invention has been described with reference to specific examples, it will be appreciated by those skilled in the art that it may be embodied in many other forms.

DATED this 9th Day of September, 2002

Attorney: JOHN B. REDFERN
Fellow Institute of Patent and Trade Mark Attorneys of Australia
of BALDWIN SHELSTON WATERS

FIGURE 1

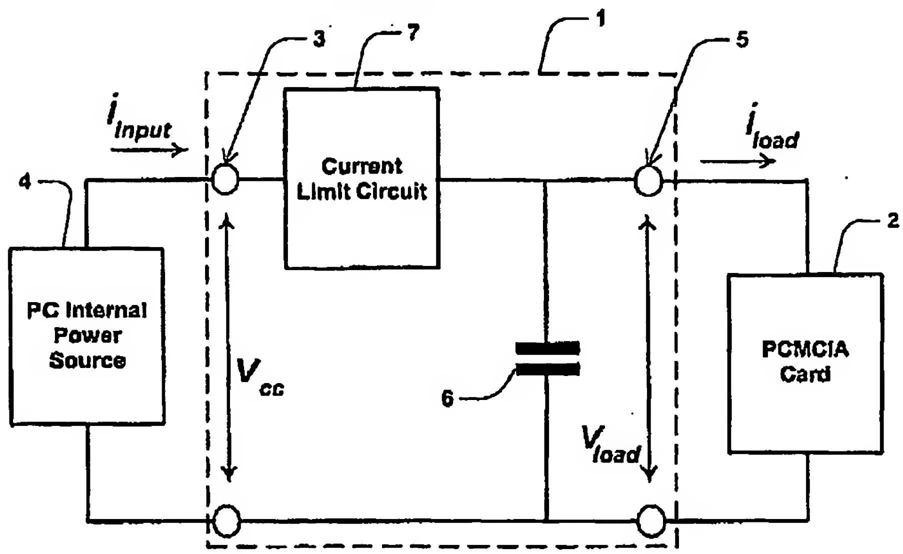

FIGURE 2

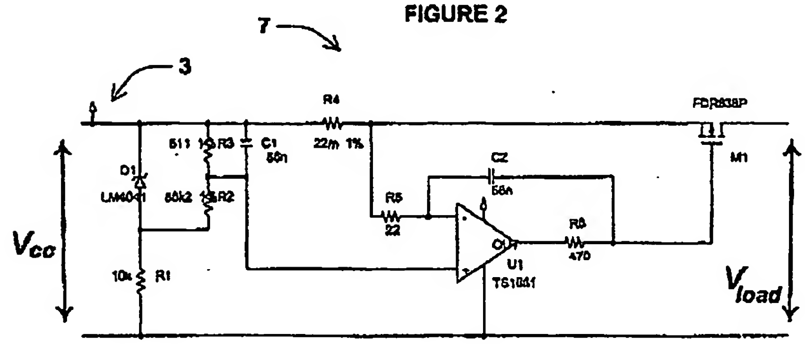

FIGURE 3

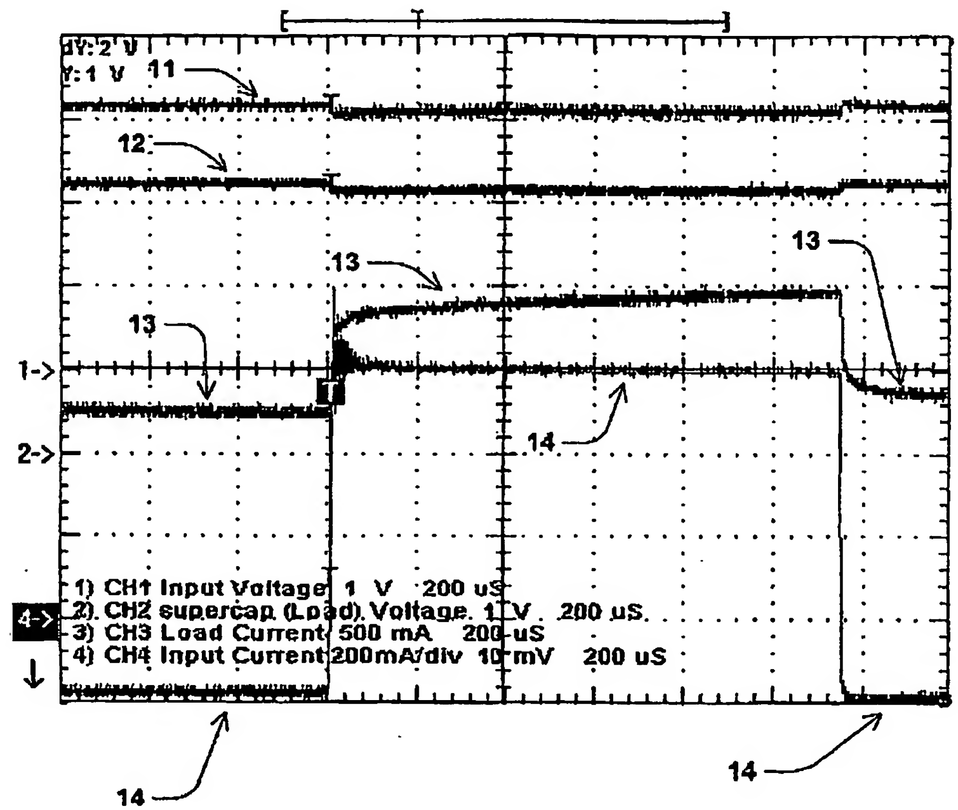
dV:2 V
V:1 V
11
12
13
13
13
14
14
14
1->
2->
4->
1) CH1 Input Voltage 1 V 200 uS
2) CH2 supercap (Load) Voltage 1 V 200 uS
3) CH3 Load Current 500 mA 200 uS
4) CH4 Input Current 200mA/div 10 mV 200 uS

FIGURE 4

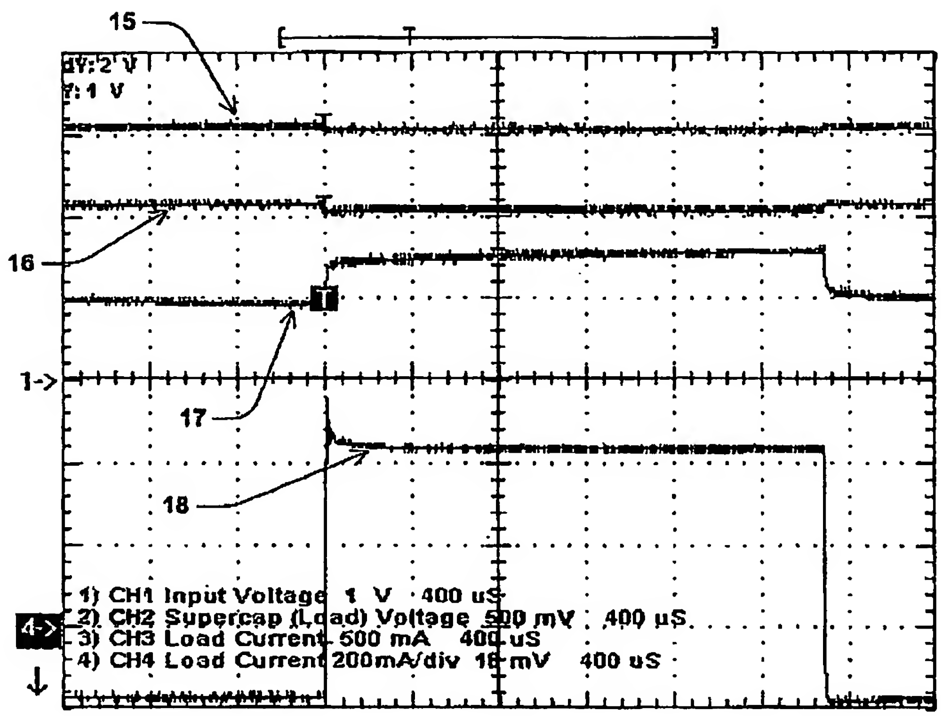
15
16
17
18
1->
4->
dV: 2 V
V: 1 V
1) CH1 Input Voltage 1 V 400 uS
2) CH2 Supercap (Load) Voltage 500 mV 400 uS
3) CH3 Load Current 500 mA 400 uS
4) CH4 Load Current 200mA/div 10 mV 400 uS

FIGURE 5

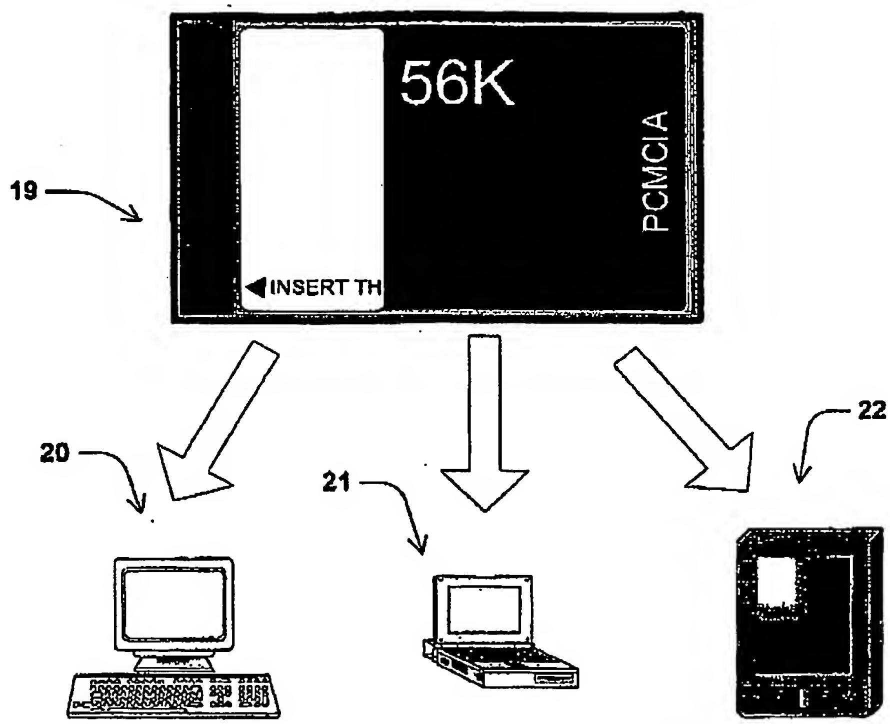

FIGURE 6